REMARKS

The Examiner's Final Office Action mailed on August 20, 2004 has been received and its contents carefully considered.

Claims 1, 3-5, 7-12, 14 and 16-20 are pending in this application. Claims 4, 5 and 14 are canceled in this Amendment without prejudice or waiver. In addition, claims 1, 3 and 12 are amended, and new claim 21 is added herein. Claims 1 and 12 remain the independent claims.

In the final Action, the Examiner rejects claims 1, 3, 5, 7-12, 14 and 16-20 under 35 USC 102(b) as being anticipated by Wu (U.S. Patent No. 6,239,007 B1), and rejects claim 4 under 35 USC 103(a) as being obvious over Wu. In this Amendment, independent claims 1 and 12 are further amended by incorporating the limitations of canceled claims 4 and 5, and claim 14, respectively, to more clearly distinguish over the applied Wu reference. Claim 3 is amended and new claim 21 is added to more clearly define the different embodiments of the invention to which the claims are directed.

The present application discloses a method for manufacturing a semiconductor device having a T type gate electrode capable of forming the wide upper gate electrode on, the lower gate electrode in a self-aligned manner without using a photolithographic step at all. Using the inventive process, it is possible to manufacture devices with a good yield and in a very simple manner. By only having to form a first insulating film and a second insulating film with the desired thicknesses, and by selectively etching the insulting films, manufacturing cost can be reduced.

In a first embodiment disclosed in the application, after forming the first insulating film to be thicker than the first polysilicon (lower gate electrode), the whole surface thereof is etched back to be thin. Thereafter, the second insulating film is formed to have such a thickness as to flatten a difference in height near the lower gate electrode.

In a second embodiment, after forming the first insulating film to be thicker than lower gate electrode and to leave a difference in height around the lower gate electrode, the second insulating film is formed to have such a thickness as to flatten a difference in height near the lower gate electrode.

The first and second embodiments differ from each other in whether or not etch back is carried out after forming the first insulating film and before forming the second

insulating film, as reflected in claims 3 and 21. The common features, defined in claims 1 and 12, are: forming the second insulating film to have such a thickness as to flatten a difference in height around the lower gate electrode; selectively etching back the second insulating film until the first insulating film on the upper surface of the lower gate electrode is exposed; selectively etching back the first insulating film to expose the upper surface of the lower gate electrode and the peripheral part of the first insulating film around the lower gate electrode to create a space in which a second polysilicon can be formed on the upper surface of the lower gate electrode. Thereby it is possible to form a wide upper gate electrode on the narrow lower gate electrode by selectively etching the insulating films.

In the first embodiment, the reason for making the thickness of the first insulating film thin by etching back after forming the first insulating film to be thick is that if the insulating film is initially formed to be thin, film thickness becomes irregular and desired electrode forms cannot be obtained uniformly across the wafer plane, resulting in lower device yields (see, for example, application page 6, lines 26-28).

In the second embodiment, where the first insulating film is formed thick and not etched back to make it thin, the difference in height of the second insulating film around the upper portion of the lower gate electrode is relaxed as compared to the first embodiment. As a result, it is possible to ensure that in the subsequent etch-back step, the first insulating film on the surface of the lower gate polysilicon will be uniformly exposing across the wafer plane, thus promoting better device yield (see, for example, application page 11, lines 19-27).

With respect to claim 4, the Examiner acknowledges in the Final Action that Wu fails to disclose the limitation, now recited in claim 1, "forming a first insulating film ... to be thicker than said first polysilicon." The Examiner argues that it would have been obvious to one of ordinary skill in the art at the time the invention was made, to form the first insulating film to be thicker than the first polysilicon, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art.

The Applicant respectfully disagrees. The limitation of claim 4 represents a difference in kind rather than degree. Figures 1A-1E in Wu all clearly disclose that

insulation layer 104 is thinner than the height of gate structure 102. There is nothing in either the figures or text of Wu to suggest the claimed limitation. Moreover, contrary to the Examiner's assertions, the claimed limitation has advantages that are not obvious from the prior art. The present application discloses two exemplary embodiments - the first in which the first insulating film is formed to be thinner than the first polysilicon and the second in which the first insulating film is formed to be thicker than the first polysilicon. It should be clear from the discussion above that both embodiments advantageously overcome certain processing irregularities to which the prior art is prone, ensuring more reliable results. Wu neither teaches nor suggests the etch-back process used to achieve the thinner first insulating film in the first embodiment, or the advantageous use of the thicker first insulating film in the second embodiment.

For at least the foregoing reasons, it is respectfully submitted that amended claims 1, 3 and 12, as well as claims 7-12 and 16-21, patentably distinguish over Wu.

The Examiner's various objections and rejections having been fully addressed, it is submitted that the application is in condition for allowance. Notice of such, with claims 1, 3, 7-12 and 16-21, is earnestly solicited.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,

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Date

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